IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: George Eckert II
Serial No.:	08/903453	Group Art Unit: 2815
Filed:	July 29, 1997	Docket: 303.378US1
Title:	CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS	

REPLY BRIEF UNDER 37 CFR 1.193(b)

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This Reply Brief is filed in triplicate and presented in response to the Examiner's Answer (the "Answer") dated March 29, 2004. The Appellants respectfully request acknowledgment of receipt, and entry of this Reply Brief in the above-identified Application for review by the United States Patent and Trademark Office Board of Patent Appeals and Interferences (the "Board").

REPLY

All of the pending claims 2, 3, 24-28, 41-48, 50-52, and 65-68 were rejected under 35 U.S.C. §103 in view of a combination of references including Sakata and Sugita. The appellant respectfully submits that the rejections of claims 2, 3, 24-28, 41-48, 50-52, and 65-68 were erroneous as argued in the appellant's Brief on Appeal (the "Brief") filed on 15 December 2003. The appellant addresses the most significant errors in the Answer herein.

I. The Rejections Are Not Supported By Evidence

The Federal Circuit has emphasized the need for the PTO to furnish evidence in support of claim rejections under 35 USC § 103 in *In re Lee* which is quoted in the Brief. The Answer states that the motivation for combining Sakata and Sugita is that:

> "the source, drain and channel regions allow individual floating gate devices to be formed in an array. That is, by forming source and drain regions having the floating gate stack there between, a plurality of floating gate devices can be formed in one substrate and yet be individually written and erased by the use of the source, drain and channel regions. The use of the source/drain/channel regions for such programming is well known in the art." Answer, page 5.

The Answer did not cite evidence in the record, such as one of the references, that supports the above-stated motivation for combining Sakata and Sugita as is required by *In re Lee*. This statement of motivation is not a quote from the applied references. The Answer stated that "the previous rejection included *seven* additional references that taught that a floating gate device needs sources and drains so that the individual devices may be formed in an array." Answer, page 11. The use of source/drain/channel regions for programming memory devices may be known in the art, but the rejection is based on the diode structure of Sakata. The Answer did not provide evidence showing the diode structure of Sakata to be similar to the other memory devices described as being "well known in the art." The Answer also did not point to a quote in the applied references to show that source, drain, and channel regions are *necessary* for individual floating gate devices to be formed in an array. The Answer has not established a *prima facie* case of obviousness without such evidence.

II. The Rejections are Based on an Improper Presumption

The rejections of claims 2, 3, 24-28, 41-48, 50-52, and 65-68 are based on the presumption that all floating gate devices are similar to that of Sugita and have the same basic structure. Sakata states that "the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices." Sakata, page 688, column 1. This is the kernel of the association between Sakata and floating gate devices. Section III of the Answer describes "Background Considerations of The Technology" beginning with the phrase "[i]n any floating gate memory device.." and proceeds to describe the workings of the floating-gate transistor of Burns which is similar to that of Sugita. Answer, pages 8-9. The Answer also describes the operation of the device of Wolf. Answer, pages 13-14. At the end of the description of the operation of Burns, the Answer states that "[t]here is nothing inventive in this manner of operation; it is fundamental to a floating gate memory device and is well known in the art." Answer, page 9. The Answer also referred to the many references of record that show a floating gate device. Answer, page 11. Later, in portion "**V. D.**," the Answer refines this presumption to mean that all floating gate devices "formed in silicon" are similar to that of Sugita and Burns and have the same basic structure, stating:

> "And as is *taught* by Sugita, Burns, etc., a floating gate device formed in silicon has its source and drain formed in the substrate." Answer, page 18.

The Answer provides no evidence that all floating gate devices formed in silicon are similar to that of Sugita or Burns or Wolf, and this presumption is not valid. The applicant presented the transistor of Lott-1 in the Brief that shows a GaAs/AlAs floating gate device structure that has a source, a drain, a gate, and a floating gate. The source, drain, and gate shown in Lott-1 are formed next to each other on a superlattice, and the floating gate of Lott-1 is on the other side of the superlattice. A barrier separates the floating gate of Lott-1 from the channel of Lott-1. The floating gate of Lott-1 is between the source and drain on one side and the channel on the other side, and separates the source and the drain from the channel. The transistor structure of Lott-1 is substantially different from that of Sugita, even though both have elements with the names source, drain, and floating gate. Lott-1 is evidence that devices categorized as floating gate devices do not necessarily have the structure of Sugita. The Answer has attempted to distinguish Lott-1 because it is not silicon-based. There is no evidence in the record that all silicon-based floating gate devices look like Sugita. In fact, the only reference in Sakata to a floating gate device is linked to the structure of Lott-1 as discussed below. The suggestion for the combination of Sakata and Sugita is based on this presumption that is not valid, and is not supported by the evidence of record.

The Answer objects to the reference in the Brief to "the heterojunction (HJ) diode structure of Sakata" as a misnomer. Answer, page 12. It is not a misnomer as Sakata calls the device a diode many times.

Absent evidence of a suggestion for the combination of Sakata and Sugita, the rejections claims 2, 3, 24-28, 41-48, 50-52, and 65-68 are improperly based on hindsight, and should be reversed.

III. The Answer Has Not Provided Evidence of a Reasonable Expectation of Success

The Answer has not provided evidence that the diode of Sakata with the source and drain of Sugita would be able to inject holes from the Si substrate into "the thin a-Si:H layer through the compositionally graded a-SiC:H layer" as described in Sakata. The Answer also has not provided evidence that the diode of Sakata with the source and drain of Sugita would be able

to inject holes "from the substrate into the a-Si:H layer through the graded a-SiC:H layer and recombine with the stored electrons" as described in Sakata. Sakata, columns 1 and 2. Evidence of a reasonable expectation of success of this type of operation of the diode of Sakata with the source and drain of Sugita has not been presented in the Answer as is required by *In re Vaeck* and *In re Lee*. The Answer has not established a *prima facie* case of obviousness without this element.

Absent such evidence, the addition of elements from Sugita to the HJ diode structure of Sakata would require a change in the basic principles under which the Sakata construction was designed to operate, and therefore the teachings of Sakata and Sugita are not sufficient to render claims 2, 3, 24-28, 41-48, 50-52, and 65-68 *prima facie* obvious under *In re Ratti*. The Answer stated that:

> "Sakata does *not* operate like Capasso. But, even if it did, such operation would not undermine the combination of Sakata with Sugita and Burns. The electron storage operation of Sakata is not altered in any means by the addition of a source and drain." Answer, page 17.

This statement is contrary to *In re Ratti*. If the device resulting from the combination of Sakata with Sugita and Burns cannot inject holes in the manner described in Sakata, then the basic principles of the operation of Sakata would be changed. The operating principles described in Sakata are very relevant to the patentability of the pending claims under 35 U.S.C. §103, and are evidence that the structure of Sakata is not similar to that of Sugita.

IV. The Answer Has Not Considered the Rebuttal Evidence

The Answer characterized the applicant's arguments regarding Capasso and Lott-1 as "tangentially related" and "too much." Answer, pages 17-18. Capasso and Lott-1 were identified in the record by the applicant as rebuttal evidence to the rejections under 35 USC § 103. The Federal Circuit has addressed the examination of claims rejected under 35 USC § 103 when rebuttal evidence is submitted in *In re Piasecki*:

> "If rebuttal evidence of adequate weight is produced,....the examiner must consider all of the evidence anew." *In re Piasecki*, 223 USPQ 785, 788 (Fed. Cir. 1984).

Quoting from *In re Rinehart* the court stated:

> "When prima facie obviousness is established and evidence is submitted in rebuttal, the

decision-maker must start over." *In re Piasecki*, 223 USPQ at 788.

The rebuttal evidence is exactly the kind of evidence required by *In re Lee*. The Answer states:

> "there is no suggestion, *anywhere* that the silicon-based device of Sakata would, or even could, form a source and drain next to the floating gate as shown in Lott-1's AlGaAs device." Answer, page 18.

Evidence of the suggestion is documented as follows. Sakata and Figure 1 of Lott-1 are linked by their reference to the same paper by Capasso. Lott-1 specifically says that the structure of Figure 1 is similar to that of Capasso. Sakata specifically says that Capasso reported similar memory devices. The connection between the transistor of Lott-1 and Sakata is documented by a reference in both to Capasso. This is evidence of a suggestion to one skilled in the art reading Capasso, Lott-1, and Sakata to use the heterojunction of Sakata in a transistor such as Lott-1's. This is the type of evidence of a suggestion that is necessary to a rejection under 35 USC §103 according to *In re Lee*. Such evidence of a suggestion is absent in the rejection of claims 2, 3, 24-28, 41-48, 50-52, and 65-68 based on Sakata and Sugita. The clear textual links between Sakata, Capasso, and Lott-1 are evidence very relevant to the patentability of the applicant's claims according to *In re Lee*, and should have been considered so by the Answer. The Answer has not considered all the evidence anew including Capasso and Lott-1 as is required by *In re Piasecki*.

CONCLUSION

The appellant respectfully submits that the rejections of claims 2, 3, 24-28, 41-48, 50-52, and 65-68 were erroneous. Reversal of those rejections is respectfully requested, as well as the allowance of all the rejected claims.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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X A return postcard.
X Reply Brief under 37 CFR 1.193(b) (in triplicate) (6 Pages).

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